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Application No. 09/708,494	Filing Date November 9, 2000	Examiner Kim Huynh	Group Art Unit 2112

Invention: SYSTEM-ON-A-CHIP STRUCTURE HAVING A MULTIPLE CHANNEL BUS BRIDGE

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In Re Application Of: **Pascal A. Nsame**

Application No.	Filing Date	Examiner	Customer No.	Group Art Unit	Confirmation No.
09/708,494	November 9, 2000	Kim Huynh	703-872-9306	2112	2612

Invention: **SYSTEM-ON-A-CHIP STRUCTURE HAVING A MULTIPLE CHANNEL BUS BRIDGE**

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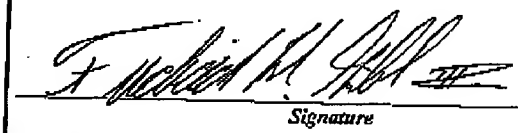

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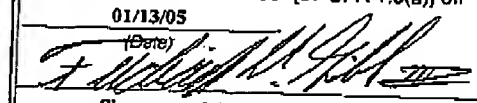

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IN THE UNITED STATES PATENT AND TRADEMARK OFFICE
BOARD OF PATENT APPEALS AND INTERFERENCES

In re Application of

Pascal A. Nsame

Serial No.: 09/708,494 Group Art Unit: 2112

Filed: November 9, 2000 Examiner: Kim Huynh

For: SYSTEM-ON-A-CHIP STRUCTURE HAVING A MULTIPLE CHANNEL BUS BRIDGE

Commissioner for Patents
P.O. Box 1450
Alexandria, VA 22313-1450

APPELLANTS' APPEAL BRIEF

Sirs:

Appellants respectfully appeal the final rejection of claims 1-29 in the Office Action dated August 17, 2004. A Notice of Appeal was timely filed on November 16, 2004.

I. REAL PARTY IN INTEREST

The real party in interest is International Business Machines Corp., Armonk, New York, assignee of 100% interest of the above-referenced patent application.

II. RELATED APPEALS AND INTERFERENCES

There are no other appeals or interferences known to Appellants, Appellants' legal representative or Assignee which would directly affect or be directly affected by or have a bearing on the Board's decision in this appeal.

III. STATUS OF CLAIMS

Claims 1-29 are all the claims pending in the application and are set forth fully in the attached Appendix. Claims 1-29 were originally filed in the application. In response to an Office Action dated May 2, 2003, Appellants filed an Amendment 1.111 on July 30, 2003, but no amendments were made to the claims. In response to the Office Action dated October 21, 2003, Appellants filed a 1.116 Amendment on December 19, 2003, however, no amendments were made to the claims. In an Interview Summary dated December 30, 2003, the Examiner stated that he would review for further clarification, and an Office Action would be forth coming. In response to the Office Action dated February 17, 2004, Appellants filed another 1.111 Amendment on May 12, 2004, amending independent claims 1 and 20. In response to the Office Action dated August 17, 2004, Appellants filed a 116 Response on October 18, 2004; however, no claim amendments were made.

Claims 1-29 stand rejected under 35 U.S.C. §102(e) as being anticipated by Swanstrom et al., hereinafter "Swanstrom" (U.S. Patent No. 5,872,942). Appellants respectfully traverse this rejection based on the following discussion

IV. STATEMENT OF AFTER-FINAL AMENDMENTS

An after-final Response that made no claim amendments was filed on October 18, 2004. An Advisory Action dated November 10, 2004 indicated that, upon filing an appeal, the Response filed on October 18, 2004 did not place the application in condition for allowance, and that the rejections of claims 1-29 would remain. The claims shown in the Appendix are shown in their amended form as of the October 18, 2004 Amendment.

V. SUMMARY OF THE INVENTION

The present invention provides a System-on-a-Chip integrated circuit structure that includes a bridge having a plurality of channels, each of which is uniquely dedicated to a different bus. See, for example, claim 1 where one channel is dedicated to the processor local bus, a second channel is dedicated to a peripheral device bus, a third channel is dedicated to a memory unit, and a fourth channel is dedicated to an input/output unit.

Appellants' Figure 2 illustrates a structure that is designed to reduce the latencies and increase communication speed on a SoC device. One difference with the structure shown in Figure 2 is the VCCA bridge 230 that has a SDRAM unit 208, an AGP unit 232, a PCI controller 224, a USB unit 214, and a SRAM unit 212 that are directly connected to the VCCA bridge and are not connected to a bus as they are in Appellants' Figure 1. As shown in Appellants' Figure 3, the bridge includes many dedicated channels 319- 325. Each dedicated channel is uniquely connected to a different functional element (such as buses, memory units, interface units, etc.) within the SoC.

The invention provides non-blocking communication through the multiple reserved lanes (e.g., channels 319-325) managed by an implicit protocol (e.g., buffers 314 and multiplexors 316). The invention avoids relying on handshaking signals that leads to blocking communications when a destination or a shared resource is overloaded.

The invention is important because, for systems interconnected through a shared bus interface, when more than two bus masters are active, the effective bandwidth of each access is significantly reduced compared to the maximum bandwidth observed when only one bus master is active. Furthermore, if concurrent accesses are not coordinated, one or more bus master may incur an unacceptable latency due to busy wait signals. This latency is even longer when access is required across a bus bridge.

By adding hardware support for non-blocking inter-virtual component communication, in the form of the VCCA bridge 230, the invention improves the performance of embedded systems. Such performance gains allow concurrent computations to utilize nearly all the available bus bandwidth while satisfying real-time requirements through the use of dedicated channels for each interface. The VCCA bridge 230 provides a performance boost on embedded systems in which there are contentions for communication resources (e.g. shared bus bandwidth, FIFO buffer) among application components.

Furthermore, the VCCA bus bridge's 230 ability to exploit a large processor local bus bandwidth is relatively independent of the processor's access pattern or the number of streams in a given computation. The VCCA bridge 230 configured with appropriate FIFO 314 depths, can generally exploit the full available processor local bus bandwidth.

VI. ISSUES PRESENTED FOR REVIEW

The issues presented for review by the Board of Patents Appeals and Interferences are whether claims 1-29 are anticipated under 35 U.S.C. §102(e) by Swanstrom. Appellants respectfully traverse these rejections.

VII. GROUPING OF THE CLAIMS

As supported by the following arguments, the claims are each independently patentable and do not stand or fall together. More specifically, the dependent claims are patently distinct from the independent claims from which they depend because each dependent claim defines additional features which are not defined in the independent claims or which are defined more broadly in the independent claims.

As discussed in greater detail below, the features defined by the dependent claims are not merely illustrations or examples but include patentable features which prevent the dependent claims from standing or falling with their associated independent claim.

VIII. ARGUMENT

A. The Prior Art Rejections

1. The Position in the Office Action

In the Office Action dated August 17, 2004, the rejections are as follows:

As per claims 1, 10, 11, 20, 21, Swanstrom discloses a system-on-a-chip integrated circuit structure comprising:

a bridge(fig.1, 106) having a plurality of channels in said bridge; (fig.1, 104,108,120, 130), (col.16, line 62-col. 17, 4) wherein each these busses comprising single or multiple channels, i.e., multimedia bus (130) comprises separate channels for different data types. (col. 4, lines 19-26);

a processor local bus connected to said bridge, wherein said bridge includes a first channel dedicated to said processor local bus (fig,1, 104); (col.7, lines 49-51) ;

at least one logic device (fig.1, 107) connected to said processor local bus; (col.3, lines 11-14);

a peripheral device bus (fig,1, 120) connected to said peripheral device bus; at least one peripheral device connected to said peripheral device bus; (col.8, lines 6-13)

at least one memory (fig.1, 110) unit connected to said bridge, wherein said bridge includes a third channel (fig.1, 108) dedicated to said memory unit; (col.4, lines 37-51); and

at least one input/output unit connected to said bridge, wherein said bridge includes a fourth channel (fig.1, 130) dedicated to said input/output unit, (col.5, lines 19-33).

As per claims 2, 12, 22, Swanstrom discloses wherein each of said channels includes buffer memories adapted to stored data when a previous data transfer is being performed. (col.24, lines 14-28) As per claims 3, 13, 23, Swanstrom discloses wherein said buffer memories comprises FIFO buffer memories, (col.24, lines 14-28), buffers inherently includes FIFO.

As per claims 4, 14, 24, Swanstrom discloses a multi-port static random access memory (SRAM) adapted to stored data when a previous data transfer is being performed. (col.24, lines 14-28).

As per claims 5,15, 25, Swanstrom discloses a multiplexor adapted to selectively connect to other channels, (col.17, lines 50-61), (col.18, lines 22-31).

As per claims 6,16, 26, Swanstrom discloses at least one memory unit comprises a first-type memory unit and a second-type memory unit different than said first-type memory unit, wherein said third channel is dedicated to said first-type memory unit and said bridge includes a fifth channel dedicated to said second-type memory unit, (col.4, lines 37-63). As per claims 7, 17, 27, Swanstrom discloses wherein said first-type memory unit comprises static random access memory (SRAM) and said second-type memory unit comprises synchronous dynamic random access memory (SDRAM), (col. 22, lines 20-37).

As per claims 8,18, 28, Swanstrom discloses at least one input/output unit comprises one or more of a peripheral interface, graphics interface, and serial bus interface, and wherein said bridge includes dedicated channels for each of said peripheral interface, graphics interface, and serial bus interface, (col.,17, line 50-col.,18, line 8).

As per claims 9,1 9, 29, Swanstrom discloses at least one peripheral device includes one or more of a serial connection, network interface connection, and

programmable input/output connection each connected to said peripheral device bus, (col.,17, line 20-Col.18, line 8).

The Office Action further stated "Appellants Amendment filed on 5/12/04 have been fully considered but are not place an application in condition for allowance. In response to Appellant's argument that with respect to the claim language distinguishing the channels in the bridge from buses channels external to the bridge provide channel(s) "in said bridge". This claim language provides that the channels are in the bridge and are therefore different than the buses/channels external to the bridge shown in figure 10 of Swanstrom, Examiner respectfully disagrees. A bridge (fig.1, 106), plurality channels (busses) (104,108,120 and 130), and furthermore, each of these buses can comprise single or multiple channels. For example, 104 dedicated for cpu 102(single) whereas the 130 (multiple channels for different data types (col.14, lines 19-26) for devices 142-146). Thus, the prior art teaches the invention as claimed and the amended claims do not distinguish over the prior art as applied."

2. Appellants' Position

a. Independent Claims 1, 10, and 20

Appellants respectfully traverse this anticipation rejection because Swanstrom is silent regarding any internal features of the bridge 106. Swanstrom merely describes the bridge 106 as being a conventional commercially available Intel bridge in column 7, lines 51-56. Therefore, Swanstrom cannot teach the claimed "channels in said bridge" defined by independent claims 1 and 20 and similarly defined by independent claim 10. Thus, as explained in greater detail below, Swanstrom does not teach each and every element of the claimed invention as defined by independent claims 1, 10, and 20 and therefore does not anticipate the invention defined by independent claims 1, 10, and 20.

The only "channels" mentioned in Swanstrom are multimedia channels 602-606 (Figure 10, column 16, line 60-column 17, line 7) which are external to the bridge 106 (and are connected to the bridge by way of buses 104, 108, 120, external to the bridge 106) and are not channels "in said bridge" as defined by independent claims 1, 10, and 20. The Office Action states that Figure 1 of Swanstrom illustrates a bridge 106 having a plurality of channels by arguing that each of the buses 104, 108, 120, and 130 can include multiple channels. However, the claimed invention is not concerned with whether the buses have multiple channels, but instead is directed to a structure having multiple channels in the bridge. In the claimed invention, the bridge (230 in Figure 2) includes multiple channels (319-325 illustrated in Figure 3). Further the claims define that each of the channels within the bridge is connected to a bus (such as the processor local bus, peripheral device bus, etc. as in claim 1). Appellants also note that there is no distinction between the bridge 106 shown in Figure 1 and the bridge 106 shown in Figure 10 of Swanstrom, and that Swanstrom merely describes the bridge 106 as being a conventional commercially available Intel bridge in column 7, lines 51-56.

It is Appellants' position that the Office Action improperly equates the channels/buses (102, 108, 120, 130, 602, 604, 605) external to the bridge shown in Figures 1 and 10 of Swanstrom with the channels (319-325) in the inventive bridge shown in Appellants Figure 3. The conventional channels that are external to the bridge do not perform the same function and are not equivalent to the claimed channels "in the bridge." Because of this and other reasons, as explained in greater detail below, it is Appellants position that the claimed invention is not taught (or even suggested by Swanstrom.

The structure in Swanstrom is similar to the structure shown in Appellants' Figure 1, where the arbiters 110, 122 restrict access to the buses 108, 120 (see page 6, line 4-page 7, line 18 of Appellants' application). With the structure shown in Appellants' Figure 1, each of the devices connected to a bus must wait for the bus to finish transmitting other data before it can transmit data over the bus (or between the buses).

This blocking increases latencies and slows the circuit's operations considerably. Appellants' Figure 2 illustrates a structure that is designed to reduce the latencies and increase communication speed on a SoC device. One difference with the structure shown in Figure 2 is the VCCA bridge 230 that has a SDRAM unit 208, an AGP unit 232, a PCI controller 224, a USB unit 214, and a SRAM unit 212 that are directly connected to the VCCA bridge and are not connected to a bus as they are in Appellants' Figure 1 and in Swanstrom. As shown in Appellants' Figure 3, the bridge includes many dedicated channels 319- 325. Each dedicated channel is uniquely connected to a different functional element (such as buses, memory units, interface units, etc.) within the SoC.

The Office Action states that Swanstrom discloses "a bridge having a plurality of channels" referring to the buses external to the bridge 104, 108, 120, 130, thereby indicating that there is no difference between the buses external to the bridge and the claimed channels in the bridge. However, Appellants submit that this interpretation is incorrect because independent claims 1, 10, and 20 explicitly distinguish between the channels in the bridge and the buses external to the bridge (e.g., independent claims 1, 10, and 20 define that the channels in the bridge are connected to different buses, which requires that the channels and the buses external to the bridge must be different components). Further, the specification (page 7, lines 13-18) explains the differences between channels in the bridge and buses connected to the bridge (e.g., see Figure 2 illustrating buses connected to the bridge and Figure 3 illustrating channels in the bridge). Therefore, as detailed below, Appellants submit that the rejection should be withdrawn.

More specifically, with respect to the claim language distinguishing the channels in the bridge from buses external to the bridge, independent claims 1, 10, and 20 provide channel(s) "in said bridge." This claim language provides that the channels are in the bridge and are therefore different than the buses external to the bridge shown in Figures 1 and 10 of Swanstrom. Further, this language of the independent claims also explains that the bus is connected to the channel, thereby again demonstrating that the channels in the bridge are different structures from the buses external to the bridge. The dependent

claims similarly define that the channels includes buffer memories, random access memory, and a multiplexor. These claims further distinguish the claimed channels from buses external to the bridge. Thus, Appellants submit that the independent claims and their dependent claims clearly provide that the channels in the bridge are not equivalent to buses external to the bridge.

As mentioned above, the specification and drawings demonstrate that the channels in the bridge are different structures from the buses external to the bridge. For example, Figure 2 illustrates many buses connected to the input/output interfaces of the bridge 230 and Figure 3 illustrates a number of buses (319-325) in the bridge. Further, page 7, lines 13-18 of the specification describe that each dedicated channel is uniquely connected to a different bus. Therefore, notwithstanding the claim language discussed above, when the claims are read in light of the specification, it is clear that the buses external to the bridge and channels in the bridge are different devices.

Thus, it is Appellants' position that the plain language of the claims and the specification defines that the channels in the bridge are different structures than the buses external to the bridge. Therefore, the Office Action's interpretation that the buses external to the bridge and channels in the bridge are equivalent is incorrect with respect to the structures defined by independent claims 1, 10, and 20. More importantly, because Swanstrom merely states that item 106 is a bridge (column 7, lines 46-62) without explaining any details of the bridge, Swanstrom cannot be said to teach or suggest different channels in the bridge being dedicated to different exterior devices as defined by independent claims 1, 10, and 20.

Further, the invention provides non-blocking communication through multiple reserved lanes in the bridge (e.g., channels 319-325) that are managed by an implicit protocol (e.g., buffers 314 and multiplexors 316). The invention avoids relying on handshaking signals that leads to blocking communications when a destination or a shared resource is overloaded. The virtual channel communication architecture (VCCA), shown in Appellants' Figures 2-4, provides application specific bus interface flow

control, by coordinating the access of resource competing components using reserved lanes. The virtual channel scheduler module uses multiple FIFO buffers 314, dedicated to distinct virtual channels 319-325, to allow the invention to implement the required multiple reserved lanes. With the invention, transactions occurring on each port interface may be routed to adjacent ports without having to pass through a bus. Similarly, each port has a data-path dedicated to the processor local bus 206.

To the contrary, Swanstrom merely describes a conventional bridge 106 and does not explain any details about the bridge 106. More specifically, in column 7, lines 46-62, Swanstrom describes that the chipset logic 106 includes various bridge logic and includes arbitration logic 107. The chipset logic 106 is similar to the Triton chipset available from Intel Corporation, including certain arbiter modifications to accommodate the real-time bus of the present invention. A second level or L2 cache memory may be coupled to a cache controller in the chipset logic 106, as desired. The bridge or chipset logic 106 couples through a memory bus 108 to main memory 110. The chipset logic 106 includes a memory controller for interfacing to the main memory 110 and also includes the arbitration logic 107. The chipset logic 106 includes various peripherals, including an interrupt system, a real time clock (RTC) and timers, a direct memory access (DMA) system, and ROM/Flash memory. Other peripherals are comprised in the chipset logic 106, including communications ports, diagnostics ports, command/status registers, and non-volatile static random access memory (NVSRAM). The host/PCI/cache bridge or chipset logic 106 also interfaces to a local expansion bus or system bus 120.

Therefore, it is Appellant's position that Swanstrom does not teach any details regarding the bridge 106 and therefore does not teach that the "bridge includes a first channel dedicated to said processor local bus . . . a second channel dedicated to said peripheral device bus . . . a third channel dedicated to said memory unit; and . . . a fourth channel dedicated to said input/output unit," as defined by independent claim 1; that the bus, memory unit, and input/output unit are each "connected to a uniquely dedicated channel in said bridge"; as defined by independent claim 10; or a bridge that has

"dedicated channels in said bridge, each uniquely connected to one or more of:" the bus, memory unit, input/output unit, and peripheral device, as defined by independent claim 20 . Therefore, Appellants submit that independent claims 1, 10, and 20 are patentable over the prior art of record. Thus, the Board is respectfully requested to reconsider and withdraw this rejection.

b. The Independent Patentability of Dependent Claims 2-9, 11-19, and 21-29

The following discussion demonstrates that Swanstrom does not teach or suggest the invention defined by the dependent claims 2-9, 11-19, and 21-29, but also that the dependent claims are independently patentable over their associated independent claims and do not stand or fall with their associated independent claims.

Claims 2, 12, and 22 define that channels in the bridge include buffer memories adapted to store data when a previous data transfer is being performed. Claims 3, 13, and 23, define that these buffer memories can comprise first-in first-out buffer memories Once again, Swanstrom merely describes the bridge 106 as being a conventional commercially available Intel bridge in column 7, lines 51-56 and does not describe any internal features regarding the bridge 106. Therefore, Swanstrom cannot disclose that the channels in the bridge include buffer memories. Further, such a feature is distinct and independent of the structure that includes multiple channels within the bridge. There is nothing within the prior art of record that would teach one ordinarily skilled in the art to include buffers within the channels in a bridge. Thus, it is Appellants' position that this feature is not taught or suggested by the applied prior art of record. Therefore, dependent claims 2, 3, 12, 13, 22, and 23 are also independently patentable over the independent claims.

Claims 4, 14, and 24 define that each of the channels includes a multi- port static random access memory (SRAM) adapted to store data when a previous data transfer is

being performed. Once again, Swanstrom merely describes the bridge 106 as being a conventional commercially available Intel bridge in column 7, lines 51-56 and does not describe any internal features regarding the bridge 106. Therefore, Swanstrom cannot disclose that the channels in the bridge include a multi- port static random access memory (SRAM). Further, such a feature is distinct and independent of the structure that includes multiple channels within the bridge. There is nothing within the prior art of record that would teach one ordinarily skilled in the art to include a multi- port static random access memory (SRAM) within the channels in a bridge. Thus, it is Appellants' position that this feature is not taught or suggested by the applied prior art of record. Therefore, dependent claims 4, 14, and 24 are also independently patentable over the independent claims.

Claims 5, 15, and 25 define that each of said channels includes a multiplexor adapted to selectively connect to other channels. Once again, Swanstrom merely describes the bridge 106 as being a conventional commercially available Intel bridge in column 7, lines 51-56 and does not describe any internal features regarding the bridge 106. Therefore, Swanstrom cannot disclose that the channels in the bridge include a multiplexor. Further, such a feature is distinct and independent of the structure that includes multiple channels within the bridge. There is nothing within the prior art of record that would teach one ordinarily skilled in the art to include a multiplexor within the channels within a bridge. Thus, it is Appellants' position that this feature is not taught or suggested by the applied prior art of record. Therefore, dependent claims 5, 15, and 25 are also independently patentable over the independent claims.

Claims 6, 16, and 26 define first-type and second-type memory units and that individual channels are uniquely dedicated to the different types of memory units. Claims 7, 17, and 27 define that the first-type memory unit comprises static random access memory (SRAM) and said second-type memory unit comprises synchronous dynamic random access memory (SDRAM). Once again, Swanstrom merely describes the bridge 106 as being a conventional commercially available Intel bridge in column 7, lines 51-56

and does not describe any internal features regarding the bridge 106. Therefore, Swanstrom cannot disclose that some of the channels in the bridge are dedicated to different external memories. Further, such a feature is distinct and independent of the structure that includes multiple channels within the bridge. There is nothing within the prior art of record that would teach one ordinarily skilled in the art to connect different channels within the bridge to different external memory units. Indeed, Swanstrom does not disclose different memory units being connected to the bridge 106, but instead merely illustrates a single memory 110 being connected to the bridge 106. Thus, it is Appellants' position that this feature is not taught or suggested by the applied prior art of record. Therefore, dependent claims 6, 7, 16, 17, 26, and 27 are also independently patentable over the independent claims.

Claims 8, 18, and 28 define that the input/output unit comprises a peripheral interface, graphics interface, and serial bus interface, and wherein said bridge includes dedicated channels for each of said peripheral interface, graphics interface, and/or serial bus interface. Claims 9, 19, and 29 define one peripheral device includes one or more of a serial connection, network interface connection, and programmable input/output connection each connected to said peripheral device bus. Claims 11 and 21 define that the bridge includes a first channel dedicated to a processor local bus; a second channel dedicated to a peripheral device bus, with different devices connected to these different buses. Once again, Swanstrom merely describes the bridge 106 as being a conventional commercially available Intel bridge in column 7, lines 51-56 and does not describe any internal features regarding the bridge 106. Therefore, Swanstrom cannot disclose that some of the channels in the bridge are dedicated to different external devices/buses. Further, such a feature is distinct and independent of the structure that includes multiple channels within the bridge. There is nothing within the prior art of record that would teach one ordinarily skilled in the art to connect different channels within the bridge to different external units. Therefore, dependent claims 8, 9, 18, 19, 28, and 29 are also independently patentable over the independent claims.

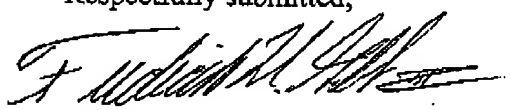
Thus, as shown above, dependent claims 2-9, 11-19, and 21-29 are similarly patentable, because they depend from claims 1, 10, and 20 and because they define novel features themselves. Thus, the Board is respectfully requested to reconsider and withdraw this rejection.

X. CONCLUSION

In view the forgoing, the Board is respectfully requested to reconsider and withdraw the rejections of claims 1-29.

Please charge any deficiencies and credit any overpayments to Attorney's Deposit Account Number 09-0456.

Respectfully submitted,



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